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Description

LINEAR-IN-DECIBEL VARIABLE GAIN AMPLIFIER

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of application of U.S. Serial number 10/708202 filed on Feb 16, 2004, which is still pending.

BACKGROUND OF INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates to a variable gain amplifier, and more particularly, to a variable gain amplifier having a linear decibel-scale gain with respect to controlling voltage(s).

[0004] 2. Description of the Prior Art

[0005] Wireless communication system development continues to rapidly progress. As a result, many kinds of high bandwidth high sensitivity transceivers have been proposed. Variable gain amplifiers are often used in this kind of

transceiver to broaden the processing range of the system. A variable gain amplifier having a linear gain in the decibel (dB) scale with respect to the controlling voltage(s) has the broadest gain range.

[0006] Please refer to Fig.1, where a circuit diagram of a conventional variable gain amplifier is illustrated. The variable gain amplifier shown in Fig.1 is a differential amplifier. The voltage gain Av of the whole circuit can be determined from the half circuit of the differential amplifier. Disregarding the phase, the voltage gain Av of this variable gain amplifier is:

[0007]
$$Av = \frac{Vout'}{Vin'} = \frac{K}{1 + \exp(\frac{Vy}{Vt})}$$

(1)

[0008] where K is substantially a constant value.

[0009] From equation (1) it can be seen that the denominator of the voltage gain Av is not a simple exponential function that it has a constant term "1" in addition to the simple exponential function exp(Vy/Vt). Consequently, the volt-

age gain Av does not have a simple exponential relationship with the controlling voltage Vy.

[0010] Please refer to Fig.2. Fig.2 is a graph showing the relationship between the voltage gain Av and the controlling voltage Vy of Fig.1. Note that when Vy < Vt, the voltage gain Av will not change exponentially with respect to the change in the controlling voltage Vy. The smaller the controlling voltage Vy is, the less the voltage gain Av will change with respect to the change in the controlling voltage Vy. The area where the voltage gain Av does not have perfect exponential relationship with the controlling voltage Vy is caused by the constant term 1 in the denominator of equation 1.

SUMMARY OF INVENTION

[0011] It is therefore one of the objects of the claimed invention to provide a variable gain amplifier having an amplifying stage and a gain controlling stage to solve the above-mentioned problem.

[0012] According to the claimed invention, a variable gain amplifier comprising: an amplifying stage and a gain controlling stage. The amplifying stage is for generating an output voltage according to a differential input voltage. The gain controlling stage is for adjusting a voltage gain of the am-

plifying stage according to a first controlling voltage and a second controlling voltage.

[0013] It is an advantage of the claimed invention that the voltage gain is inversely proportional to a simple exponential function, and the value of the simple exponential function is determined by the difference between the first and the second controlling voltages.

[0014] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0015] Fig.1 is a circuit diagram of a variable gain amplifier of the prior art.

[0016] Fig.2 is a graph showing the relationship between the voltage gain Av and the controlling voltage Vy of Fig.1.

[0017] Fig.3 is a diagram of a variable gain amplifier according to the present invention.

[0018] Fig.4 and Fig.5 are circuit diagrams of the gain controlling stage 304 according to present invention.

[0019] Fig.6 is a graph for showing the relation between the voltage gain Av and the difference between the first and the

second controlling voltages according to equation 8.

DETAILED DESCRIPTION

[0020] Please refer to Fig.3 showing a schematic diagram of a variable gain amplifier according to the embodiment of the present invention. The variable gain amplifier 300 comprises an amplifying stage 302 for generating an output voltage Vout according to an input voltage Vin and a gain controlling voltage V_y. A voltage gain, i.e. the ratio between the output voltage Vout and the input voltage Vin, is determined by the gain controlling voltage V_y. A gain controlling stage 304 is for generating the gain controlling voltage Vy.

[0021] In this embodiment, the amplifying stage 302 is the same as the variable gain amplifier shown in Fig. 1. Concerning the amplifying stage 302 please refer to Fig.1 and the above description describing the variable gain amplifier shown in Fig.1. Referring to equation 1, it can be seen that the value of the voltage gain of the amplifying stage 302 is determined by the gain controlling voltage Vy.

[0022] Next, please refer to Fig.4 and Fig.5, where circuit diagrams of the gain controlling stage 304 according to the embodiment of the present invention are illustrated. The gain controlling stage 304 is for determining the value of

the gain controlling voltage Vy output to the amplifying stage 302 according to the first controlling voltage V1 and the second controlling voltage V2. In this embodiment, the gain controlling stage 304 comprises a transconductance unit 401, a first current transforming unit 403, a second current transforming unit 405 (as shown in Fig.4), and an outputting unit 407 (as shown in Fig.5).

[0023] The transconductance unit 401 comprises a first transistor 472 coupled to the first controlling voltage V1, a second transistor 473 coupled to the second controlling voltage V2, a first bias current source Ibias1 coupled to the emitter of the first transistor 472 and the emitter of the second transistor 473 for providing a first bias current Ibias1, a first current source 402, a first resistor R1 coupled between the collector of the first transistor 472 and the first current source 402, and a second resistor R2 coupled between the collector of the second transistor 473 and the first current source 402.

[0024] The value of the first current I1 flowing through the collector of the second transistor 473 is determined by the first bias current Ibias1 and the difference between the first controlling voltage V1 and the second controlling voltage V2. In this embodiment, the relationship is as fol-

lows:

[0025]
$$I1 = Ibias1/[1 + \exp(\frac{V1 - V2}{Vt})]$$

(2)

[0026] Because the transconductance unit 401 is a differential circuit, the collector current of the first transistor 472 is determined by the first controlling voltage V1, the second controlling voltage V2 and the first bias current Ibias1. The relationship is similar to that shown in equation 2.

[0027] The first current transforming unit 403 is coupled to the transconductance unit 401 through the second current source 404. The first current transforming unit 403 comprises a third transistor 474 having the collector and the base being coupled together, a fourth transistor 475, a second bias current source Ibias2 coupled to the emitter of the third transistor 474 and the emitter of the fourth transistor 475 for providing a second bias current Ibias2, a second current source 404, a third resistor R3 coupled between the collector of the third transistor 474 and the second current source 404, and a fourth resistor R4 coupled between the collector of the fourth transistor 475 and the second current source 404. The second current

source 404 and the first current source 402 form a current mirror circuit. And in this embodiment the ratio between the collector current I2 of the third transistor 474 and the collector current I1 of the second transistor 473 is the same as the ratio between the first bias current Ibias1 and the second bias current Ibias2, as follows:

[0028] $I2 / I1 = Ibias2 / Ibias1$ (3)

[0029] Because the first current transforming unit 403 is also a differential circuit, according to the currents relationship shown in equation 3, the ratio between the collector current of the fourth transistor 475 and the collector current I2 of the third transistor 474 is the same as the ratio between the collector current of the first transistor 472 and the collector current I1 of the second transistor 473. In this embodiment, when the first bias current Ibias1 equals the second bias current Ibias2, the collector current of the first transistor 472 will also be equal to the collector current of the fourth transistor 475, and the collector current I1 of the second transistor will be equal the collector current I2 of the third transistor.

[0030] The second current transforming unit 405 comprises a fifth transistor 476 having the base and the collector coupled to the base of the fourth transistor 475, a sixth tran-

sistor 477 having the base coupled to the base and the collector of the third transistor 474, and a ninth transistor 480 coupled to the emitter of the fifth transistor 476 and the emitter of the sixth transistor 477 for providing a third bias current Ibias3. By way of the loop formed with the third transistor 474, the fourth transistor 475, the fifth transistor 476, and the sixth transistor 477, the ratio between the collector current I3 of the sixth transistor 476 and the collector current I2 of the third transistor 474 is the same as the ratio between the third Ibias2 and the first bias current Ibias1. This is shown in the following equation:

[0031] $I3 / I2 = Ibias3 / Ibias2$ (4)

[0032] The second current transforming unit 405 is also a differential circuit. As shown in the relationship between the collector current I2 of the third transistor 474 and the collector current I3 of the sixth transistor 477 shown in equation 4, the ratio between the collector current I4 of the fifth transistor 476 and the collector current I3 of the sixth transistor 477 is the same as the ratio between the collector current of the fourth transistor 475 and the collector current I2 of the third transistor 474.

[0033] Hence, according to equations 2, 3, 4, and the relation-

ship between I4 and I3 described above, the circuit shown in Fig.4 is a voltage controlled current amplifier. By way of changing the value of the differential input voltage, i.e. the difference between the first controlling voltage V1 and the second controlling voltage V2, the relationship between the output currents I3 and I4 can be controlled. The relationship is as follows:

[0034]

$$\frac{I4}{I3} = K \cdot \exp\left(\frac{V1 - V2}{Vt}\right)$$

(5)

[0035] The outputting unit 407 shown in Fig.5 comprises a seventh transistor 478 having the base and the collector being coupled together, an eighth transistor 479, and a fourth bias current source I4 coupled to the emitter of the seventh transistor 478 and the emitter of the eighth transistor 479. Please note that the voltage controlled current amplifier shown in Fig.4 is coupled to the outputting unit 407 shown in Fig.5 through at least a current mirror device (not shown), such that the bias current output by the fourth bias current source is substantially the same as the collector current I4 of the fifth transistor 476, and the col-

lector current I3 of the sixth transistor 477 is substantially the same as the collector current I3 of the seventh transistor 478. Although the current mirrors are not shown, a person skilled in the art can easily design such the at least one current mirror. At this point, the collector current of the seventh transistor 478 will be equal to the collector current I3 of the sixth transistor 477, and the collector current of the eighth transistor 479 will be equal to difference between the collector current I4 of the fifth transistor 476 and the collector current I3 of the sixth transistor 477. The base of the seventh transistor 478 and the base of the eighth transistor 479 are for coupling to the amplifying stage 302 and outputting the gain controlling voltage Vy. Hence, the relationship of the gain controlling voltage Vy, the collector current I3 of the seventh transistor 478 and the collector current (I4-I3) of the eighth transistor 479 is follows:

[0036]
$$Vy = Vt \cdot \ln\left(\frac{I4 - I3}{I3}\right) = Vt \cdot \ln\left(\frac{I4}{I3} - 1\right)$$

(6)

[0037] Accordingly, the gain controlling stage 304 is for determining the current relation in each stage of the differen-

tial circuit according to the difference between the first controlling voltage V1 and the second controlling voltage V2, and for determining the value of the gain controlling voltage Vy according to these current relations. Consequently, the relationship between the gain controlling voltage Vy, the first controlling voltage V1 and the second controlling voltage V2 is as follows:

[0038]

$$Vy = Vt \cdot \ln\left[K \cdot \exp\left(\frac{V1 - V2}{Vt}\right) - 1\right]$$

(7)

[0039] Using the gain controlling voltage Vy output by the gain controlling stage 304 as the controlling voltage Vy of the amplifying stage 302 shown in Fig.1, the voltage gain of the amplifying stage 302, i.e. the ratio between the output voltage Vout and the input voltage Vin, is as follows:

[0040]

$$Av = \frac{Vout}{Vin} = \frac{K1}{\exp\left[K2(V1 - V2)\right]}$$

(8)

[0041] where K1 relates to the output resistance RL of the amplifying stage 302, and K2 relates to the thermal voltage Vt

of bipolar junction transistors. In this embodiment, both K1 and K2 are constants.

[0042] Please note that the above-mentioned gain controlling stage 304 is only an embodiment example and the present invention is not constrained by this embodiment. Any circuit that can generate a gain controlling voltage Vy which is proportional to ln(Ia/Ib-K3) can be used to be one of the embodiments of the present invention. In this formula, K3 is a constant, Ia corresponds to the first controlling voltage V1, and Ib corresponds to the second controlling voltage V2.

[0043] It can be seen from equation 8 that through the gain controlling stage 304, the relationship between the voltage gain Av of the amplifying stage 302 and the difference between the first controlling voltage V1 and the second controlling voltage is a simple exponential function K1/exp[K2(V1-V2)]. Please refer to Fig.6. Fig.6 is a graph showing the relationship between the voltage gain Av and the difference between the first and the second controlling voltages according to equation 8. Compare Fig.6 to the graph shown in Fig.2 and it can be seen that in Fig.6 the voltage gain Av has a simple exponential relationship with the difference between the first controlling voltage

V1 and the second controlling voltage V2. That is, the denominator of the voltage gain Av is a simple exponential function, which can be expressed in the form of exp(V1-V2). Therefore, the voltage gain Av has a simple exponential relationship with the controlling voltage Vy, which is determined by the difference of the first and the second controlling voltage (V1-V2). In addition, in this embodiment, the variable gain amplifier has two input ends for receiving differential input voltage, however, the variable gain amplifier of the present invention can also be single ended in addition to the differential configuration for generating a differential output voltage.

[0044] Of course, the amplifying stage used in the present invention does not necessary need to be the same as that shown in Fig.1. Any amplifying circuit having a voltage gain with a denominator combined by a constant term and a simple exponential function term as the amplifying circuit shown in Fig.1 can be used in the present invention.

[0045] Those skilled in the art will readily observe that numerous modification and alternation of the device may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.